REMARKS

Applicants thank the Examiner for the thorough consideration given the present application. Claims 1-13 are currently being prosecuted. The Examiner is respectfully requested to reconsider his rejections in view of the remarks as set forth below.

Entry of Response

Applicants request that the present response be entered and given full consideration. Since only remarks are being presented, entry of the response is considered appropriate.

Rejection under 35 U.S.C. 112

Claims 1, 7 and 10 stand rejected under 35 U.S.C. 112, first paragraph as failing to comply with the written description requirement. The Examiner believes that the specification teaches that the system source can be readjusted according to the flow rate, but does not teach the redeployment of the whole system resource.

Applicants submit that the Examiner is incorrect in his understanding of the device. Paragraph [0020] of the present specification makes it clear that there is a preset sequence determined by the default configuration set in the motherboard during the time of manufacture. Moreover, the sequence of this priority can be changed due to the performance control chip. Accordingly, if the AGP card, which normally has a lower priority than the CPU, is busy while the CPU is not busy, the performance control chip will promote the priority of the AGP device in order to provide system source for the AGP device.

Thus, the default configuration stored in the register of the North and South bridge chips can be readjusted to change the priority of each device to share the system resource. This means that the whole system resource shared by all the devices on the motherboard is readjusted according to the full rate and not just the partial or unused resources. In view of this, Applicants submit that Examiner's rejection under 35 U.S.C. 112, first paragraph should be removed.

Rejection under 35 U.S.C. 103

Claims 10-13 stand rejected under 35 U.S.C. 103 as being obvious over Iwazaki (U.S. Patent 6,073,244) in view of Messick et al. (U.S. Published 2004/0044770). This rejection is respectfully traversed.

The Examiner states that Iwazaki teaches a method for adjusting the system performance of the computer including the steps of executing a program or measuring a flow rate of data, defining a predetermined flow rate, repeating the steps, measuring actual data flow rates of motherboards, ascertaining the operating states of all the devices and comparing the operating states adjusting the operating rates of each device. The Examiner admits that Iwazaki fails to teach the redeploying of the whole system resource shared by all the devices. The Examiner relies on Messick to teach the method of managing system resource allocation in an apparatus that receives a plurality of requests from a plurality of devices. Messick teaches monitoring the activity at each port, comparing the operating state of all the devices, and redeploying whole system resources shared by all the devices.

Applicants submit that it would be improper to try to combine the device of Iwazaki with the device of Messick. Messick has disclosed a method for managing bandwidth allocation in a storage area network that receives I/O requests from a plurality of client devices and determines the priority of client device. However, in the present invention, the method adjusts the system performance on the computer, especially for monitoring the actual data flow rates of devices fabricated on a motherboard and adjusting the operating rates of those devices. It is clear that the method of Messick is designed for the storage area network and the bandwidth shared by the remote client devices which is not the same as a method of monitoring and deploying the resource shared by devices fabricated on a motherboard. Accordingly, Applicants submit that it not would be obvious to combine the references and that it is not clear that such device would be operational.

Claims 1, 2, 4, 6-8 and 10-12 stand rejected under 35 U.S.C. 103 as being obvious over Filippo (U.S. Patent 6,976,182) in view of Jacobson (U.S. Patent 6,915,518) or Messick. This rejection is respectfully traversed.

The Examiner states that Filippo teaches an apparatus for adjusting the system performance of the computer having a plurality of performance monitor means, a performance control chip which is capable of ascertaining whether the operating state of each device is busy or not. The Examiner admits that Filippo does not teach the redeploying of a whole system resource shared by all the devices.

The Examiner relies on Jacobson to teach a system directed the run time reallocation of resources in response to changing activity level. In particular, Jacobson teaches a load monitor coupled to the PLDs for monitoring the activity level of the functions. Messick teaches another method for dynamically reallocating bandwidth resource in response to the activity measure at each port. The Examiner feels it would have been obvious to combine the teachings of either Jacobson or Messick with Filippo in order to prove the system performance by providing the system with the ability to dynamically optimize the whole resource shared by all the devices.

Applicants disagree with the Examiner's combination of these references. The apparatus proposed by Filippo relates to a microprocessor, the integer execution unit and the floating point execution unit which are different from the devices fabricated on a motherboard such as the CPU, the north and south bridge chips, the AGB, the PCI and the motherboard power supply. Applicants submit that this arrangement differs from that of the present invention and that an arrangement can not be applied against a device such as described in the present application. Likewise, it is also not clear that the references can be combined since they also relate to different devices. Accordingly, Applicants submit that these claims are allowable over this rejection.

Furthermore, regarding claims 2 and 8, the Examiner feels that it would be obvious that the generic bus line of Filippo encompasses any well known claimed bus lines such as the PCI bus line, the AGP bus line or the RAM bus line and the CPU bus line. Applicants disagree with

this statement and believe that since Filippo has disclosed a microprocessor, the lines for connecting the integer execution unit, the floating point execution unit, the integer activity detecting unit and the floating point activity detector unit can only be connected using an interconnection line formed in the microprocessor and it is unlikely to be the bus lines such as the recited PCI, AGP, RAM or CPU bus lines. Accordingly, Applicants submit that these are claims are additionally allowable.

In regard to claim 6, the Examiner felt that Filippo teaches that the performance control chip is connected to a power supply that is capable of controlling the operating rate of the device by adjusting the power supply thereto. However, columns 6, lines 40-52 of Filippo clearly indicate that control unit 102 determines if a functional unit 104 is or will be inactive so that is may disable the power to the functional unit. When the control unit determines that actively will resume for its functional unit, it enables power thereto. Thus, the activity detector and power control unit proposed by Filippo is applied to monitoring and determining the future state of the functional units and whether they would be active or inactive and to either provide power or shut power off to the units. This means that the activity detector and power control unit is unlikely to be used for adjusting the power supply to the functional units in order to control the operating rate thereof as proposed by the present claimed invention. Accordingly, Applicants submit that claim 6 is additionally allowable.

Claims 10-13 stand rejected under U.S.C. 103 as being obvious over Gunther (U.S. Patent 5,781,783) in view of Jacobson or Messick. The Examiner states the Gunther teaches an apparatus for adjusting the system performance of a computer including a plurality of performance monitor means and a performance control chip for adjusting the operating rate of the devices. The Examiner admits that Gunther does not teach the redeployment of the whole system resource shared by all the devices. Jacobson and Messick teach other systems for reallocation of resources as described above. Applicants submit that the claims are not obvious over this combination of references. However, the Gunther reference teaches at column 7, lines 1-6 that the control circuit includes activity monitoring logic 62 which monitors the activity of the BIU 32 and provides a signal for each clock cycle when the BIU is active and a second signal

reaches clock cycle in which the BIU is inactive. Also, column 8, lines 64 and following recite that the control circuit 84 is arranged to power down the L2 memory 82 when a number of the L1 memory 80 hits corresponding to the first threshold have occurred and then power up the memory 82 when a number of memory 80 hits correspond to the second threshold has occurred. Thus, it is clear that the control 60 disclosed by Gunther is not applied to adjust the operating rate of the device but instead is applied to monitor and determine that the BUI is active or inactive and then power up or power down the device in order to save power.

Further, Applicants submit that the apparatus proposed by Gunther is in regard to a processor and the devices are the circuit blocks fabricated in the processor. This is described in column 6, lines 59-62 wherein the application of the present invention to the circuit blocks and sub circuit blocks is described. Apparently, these circuit blocks are all fabricated in the processor and are different from devices fabricated on the motherboard such as the CPU, the north and south bridge chips, the AGP slot, the PCI slots and the motherboard power supply. Accordingly, Applicants submit that these claims are allowable over the combination of references cited by the Examiner.

In regard to claims 2 and 8, the Examiner believes that Gunther teaches bus lines including a CPU bus line. However, based on the above description, the circuit blocks of Gunther, and the circuit which are to monitored and readjusted are all the elements formed in processor. This means that the lines to be monitored are still the interconnection lines formed in the processor and are unlikely for Gunther to monitor bus lines such as the PCI, AGP, RAM and CPU bus lines. Accordingly, these claims are additionally allowable.

Similarly, in regard to claims 3, 9 and 13, the devices that Gunther wants to monitor and readjust are all circuit blocks formed in the processor which are different from the device proposed by present invention. In addition, Applicant submits that combining Jacobson or Messick with or Iwazaki, Filippo or Gunther are contrary to the teachings of the Iwazaki, Filippo and Gunther references. Messick teaches dynamically allocating bandwidth resources to each client device based on the priority assigned to that device. Jacobson teaches reallocating the PLD resources between the various functions in proportion to increasing or decreasing activity levels.

It is noted that the object of Iwazaki, Filippo and Gunther is to provide an apparatus or method for reducing electric power conception, whereas modifying these in accordance with the teachings of Jacobson or Messick would not reduce the power consumption. Accordingly, Applicants submit that a modification would render the devices unsatisfactory for their intended use. According, a modification would be suggested.

Conclusion

In view of the above remarks, it is believed that the claims clearly distinguish over the patents relied on by the Examiner, either alone or in combination. In view of this, reconsideration of the rejection and allowance of the claims are respectfully requested.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Robert F. Gnuse Reg. No. 27,295 at the telephone number of the undersigned below, to conduct an interview in an effort to expedite prosecution in connection with the present application.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37.C.F.R. §§1.16 or 1.14; particularly, extension of time fees.

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Respectfully submitted,

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